I. Amendments to the Claims

1. (Currently Amended) An integrated test circuit arrangement

having integrated test structures located on a integrated circuit substrate,

at least one integrated heating element located on the integrated circuit substrate,

an integrated detection unit, located on the integrated circuit substrate, which detects at least one physical property for each of the test structures,

an integrated supply unit, located on the integrated circuit substrate, which supplies each of the test structures with a current or a voltage in switchable fashion independently of one another, and

a control unit which is connected to outputs of the detection unit on an input side and which controls the supply unit dependent on the detection results.

2. (Cancelled)

3. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein the test structures of a first group have the same construction among one another.

4. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein at least one of:

the supply unit contains at least one of: a multiplicity of integrated current sources and a multiplicity of integrated voltage sources, and

the current sources contain a plurality of current mirrors which each generate a multiple or a fraction of a reference current or a current having the magnitude of the reference current.

5. (Currently Amended) The circuit arrangement as claimed in claim [[2]] 1, wherein the heating element at least one of:

contains a resistance heating element which comprises monocrystalline silicon or polycrystalline silicon or which comprises a metal, and

has a straight profile, a meandering profile, a triangular function profile or a rectangular function profile.

6. (Previously Presented) The circuit arrangement as claimed in claim 1, further comprising at least one reference structure, at least one of the construction and the dimensions of which differ from the construction and the dimensions of the test structures.

7. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein the detection unit at least one of:

is connected or can be connected to the test structures, and

contains at least one counter unit, which is clocked in accordance with a predetermined clock.

8. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein at least one of:

the detection unit contains at least one multiplexer unit, the inputs of which are electrically connected to a respective test structure, and

an output of the multiplexer unit is connected to a first input of a comparison unit, a second input of which is electrically connected to a reference structure, the reference structure having at least one of a different construction and different dimensions than the test structures.

9. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein the control unit outputs at least one of: detection results, a datum for ascertaining the detection instant and a datum for identifying the test structures.

10. (Cancelled)

11. (Previously Presented) The circuit arrangement as claimed in claim 1, further comprising electronic components associated with a user circuit.

12. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein the circuit arrangement is encapsulated in a plastic housing or in a ceramic housing.

13. (Previously Presented) A method for testing test structures, the method comprising the following steps that are implemented without limitation by the order specified:

integrating test structures into an integrated circuit arrangement,

integrating a detection unit into the integrated circuit arrangement, the detection unit detecting at least one physical property of the test structures,

integrating at least a part of a supply unit into the integrated circuit arrangement,

connecting the test structures to the supply unit,

detecting one of the physical properties of each of the test structures by means of the detection unit, and

integrating a control unit into the integrated circuit arrangement, which is connected to outputs of the detection unit on an input side and which controls the supply unit dependent on the detection results.

14. (Previously Presented) The method as claimed in claim 13, further comprising at least one of the following steps:

integrating at least one heating element into the integrated circuit arrangement,

warming or heating the test structures with the aid of the heating element, and

connecting the supply unit to the test structure during warming or during heating.

15-16. (Cancelled)

17. (Previously Presented) The method as claimed in claim 13 further comprising the following steps:

integrating at least one reference structure, at least one of the construction and the dimensions of which differ from the construction and the dimensions of the test structures,

detecting one of the physical reference properties at the reference structure,

comparing the one of the physical properties with a reference property or comparing a quantity generated from the one of the physical properties and a quantity generated from the reference property.

18. (Previously Presented) The method as claimed in claim 13, wherein the same physical properties of different test structures are successively compared with a reference property.

19. (Previously Presented) The method as claimed in claim 14, wherein the heating element is at least one of:

fed with at least one of an AC current and a DC current, and

heated to temperatures of greater than two hundred degrees Celsius.

20. (Previously Presented) The method as claimed in claim 13, wherein an output circuit is integrated into the integrated circuit arrangement, the output circuit outputs at least one set of detection data for the test structures.

21. (Previously Presented) The method as claimed in claim 13, wherein the method is implemented at least one of:

with an unencapsulated integrated circuit arrangement,

with an integrated circuit arrangement that is still arranged on a semiconductor wafer, the semiconductor wafer carrying a multiplicity of other integrated circuit arrangements, and

for the purpose of monitoring ongoing production.

22. (Previously Presented) The method as claimed in claim 13, further comprising integrating at least a part of the supply unit into the integrated circuit arrangement, said part containing at least one active component.

23. (Currently Amended) The circuit arrangement as claimed in claim [[2]] 1, wherein:

the test structures of a second group contain interconnects which at least one of: comprise a metal or are led into another metallization layer by means of a via,

the test structures of a third group contain dielectrics, or

the test structures of a fourth group contain active or passive electronic components.

24. (Previously Presented) The circuit arrangement as claimed in claim 11, wherein the electronic components comprise at least one of a memory unit and a processor.

25. (Previously Presented) The method as claimed in claim 17, further comprising registering an instant at which the comparison result changes.